SELECTIVE PHOTORESIST HARDENING TO FACILITATE LATERAL TRIMMING

ABSTRACT OF THE DISCLOSURE

A process for forming sub-lithographic features in an integrated circuit is disclosed herein. The process includes modifying a photoresist layer after patterning and development but before it is utilized to pattern the underlying layers. The modified photoresist layer has different etch rates in the vertical and horizontal directions. The modified photoresist layer is trimmed with a plasma etch. A feature included in the trimmed photoresist layer has a sub-lithographic lateral dimension.